CLAIMS:

1. Apparatus (20; 30; 41) for performing a temperature measurement function, comprising a first stage with

- a first circuit (11) and a second circuit (12) being arranged in parallel,
  - said first circuit (11) comprising a first transistor (M1), a first resistor (R_{temp}), and a parallel arrangement of n diodes (B1 – Bn),
  - said second circuit (12) comprising a second transistor (M2) and a parallel arrangement of m diodes (C2),
- an operational amplifier (13) on the input side being connected to the first circuit (11) and the second circuit (12), said operational amplifier (13) applying a gate voltage to said first transistor (M1) and said second transistor (M2),

said apparatus (20; 30; 41) further comprising an output stage with p output transistors (N1 - Np), and an output resistor ($r*R_{temp}$) performing a current to output voltage conversion in order to provide an output voltage ($V_{tempout}$) that depends on the actual temperature (T).

2. The Apparatus (20; 30; 41) of claim 1, wherein said first transistor (M1) provides a first current (I1) flowing through the parallel arrangement of n diodes (B1 – Bn) and said second transistor (M2) provides a second current (I2) flowing through the parallel arrangement of m diodes (C2).

3. The Apparatus (20; 30; 41) of claim 1 or 2, wherein said operational amplifier (13) has a first input (15), a second input (14), and an output (16), the first input (15) being connected to a drain of the first transistor (M1) and the second input (14) being connected to a drain of the second transistor (M2), said output (16) being connected to a gate of said first transistor (M1) and a gate of said second transistor (M2) for biasing these transistors (M1, M2).

4. The Apparatus (20; 30; 41) of claim 1 or 2, wherein said output stage amplifies said first current (I1) to obtain a third current (I3) before performing said current to output voltage conversion by converting said third current (I3) into said output voltage ($V_{tempout}$).

5. The Apparatus (20; 30; 41) of claim 1 or 2, wherein said first resistor (R_{temp}) and said output resistor ($r*R_{temp}$) are both either integrated Npoly resistors or integrated Ppoly resistors.

6. The Apparatus (20; 30; 41) of claim 1, 2 or 5, wherein said output resistor ($r*R_{temp}$) is realized by a plurality of r resistors, the resistance of the output resistor ($r*R_{temp}$) being r times the resistance of said first resistor (R_{temp}), r being an integer number.

7. The Apparatus (20; 30; 41) of claim 1, 2 or 3, comprising a hold-capacitor (C) being arranged in parallel to the output resistor ($r*R_{temp}$) in order to filter out noise and/or to stabilize said output voltage (Vt_{empout}).

8. The Apparatus (20; 30; 41) of claim 1, 2 or 3, wherein said first transistor (M1) and said output transistors (N1 - Np), as well as said first resistor (R_{temp}) and output resistor ($r*R_{temp}$) are designed to minimize mismatch effects.

9. The Apparatus (20; 30; 41) of one of the preceding claims, wherein said number n, m and p are integer numbers.

10. The Apparatus (20; 30; 41) of one of the preceding claims, wherein diode-connected PNP bipolar transistors (B1 – Bn, C2) serve as diodes.

11. The Apparatus (20; 30; 41) of one of the preceding claims, wherein said operational amplifier (13) is a low-offset operational amplifier.

12. The Apparatus (20; 30; 41) of one of the preceding claims, wherein the output voltage ($V_{tempout}$) and the actual temperature (T) have a linear dependency.

13. The Apparatus (20; 30; 41) of one of the preceding claims, wherein the gate voltage is applied to gates of the p output transistors (N1 - Np).

14. The Apparatus (30) of one of the preceding claims further comprising a temperature compensation network (31) providing a bandgap reference voltage (V_{bgp}) at another output (36).

15. The Apparatus (30) of claim 14, wherein the temperature compensation network (31) comprises a plurality of voltage followers (32, 33, 34) with an implemented offset, the voltage followers (32, 33, 34) being connected in series.

16. Device (40) comprising an apparatus (41) according to one of the claims 1 through 15.

17. The device (40) of claim 16, further comprising an analog-to-digital converter (42).

18. The device (40) of claim 16 being part of an analog, a mixed-mode, or a digital device.